INDIAN INSTITUTE OF INFORMATION TECHNOLOGY
DESIGN AND MANUFACTURING (IIITDM) KANCHEEPURAM

INTRODUCTION OF NEW COURSE

Course Title	**SOC Low Power design and verification**	Course Code	EC5XXX			
Dept./ Specialization	ECE	Structure (LTPC)	3	0	2	4
To be offered for	DD/M.Tech	Status	Core ☐		Elective ▬	
Faculty Proposing the course	Hariharan Seshadri	Type	New ▬		Modification ☐	
Recommendation from the DAC		Date of DAC				
External Expert(s)						
Pre-requisite	Detailed below this table	Submitted for approval			47th Senate	
Learning Objectives	• Understand Low Power design issues, challenges • Understand Low Power design optimization techniques • Understand how to verify low power designs					
Learning Outcomes	• Skill on low power needs at various design stage from architecture to implementation • Ability to write power intent in UPF format • Familiarly with usage of Cadence Low power flows					
Contents of the course *(With approximate break-up of hours for L/T/P)*	• Introduction, need for low power, components of power, levels of abstraction for power optimization, power estimation, power verification techniques, role of device technology (2L, 0P) • Algorithmic and Architectural level power optimization: area, performance, power trade-offs, case studies, design considerations for low power CPU design (8L, 0P) • Power optimization at RTL design phase: components of total power, clock gating, power domains, level shifter, clamps, power switches, power gating, retention concepts, split rail memory, DCVS, frequency and voltage scaling, low power modes, concept of PMU, PMIC, LDO (8 L, 0P) • Power estimation at RTL: Importance of estimating power early in design cycle, Cadence Joules flow and methodology (4 L, 2P) • Introduction to UPF: what is UPF, components of UPF: power domain, power supply network, power state tables, retention strategies, isolation strategies, level shifter strategies (10L, 0P) • Power verification: static and dynamic: Introduction to low power lint structural verification, Conformal Low Power, Power aware formal verification, Introduction to low power verification and power aware simulation. Challenges in power aware verification. A Case study of low power verification of CPU sub system (6L and 8P) • Power optimization at implementation: various logic optimization techniques, how EDA tools help to save power during implementation (4L and 4P) • (Note – breakup of number of lectures and lab is initial estimate, can finalize once course material is prepared, as there are no standard text books meeting industry requirements.)					
Text Book	1. Low power design methodologies: Jan M. Rabay and Masssoud Pedrum, Kulwar Academic Publishers 2. High level power analysis and optimization: Anand Raghunathan and Niraj jha, Suraj Dubey, Springer science and business media: ISBN 978-1-4615-5433-2					
Reference Books	1. IEEE Standard for Design and Verification of Low-Power, Energy-Aware Electronic Systems - IEEE 1801-2018 2. Cadence user manual for Joules, Conformal LEC, Conformal Low Power, Genus					

technology libraries characterized for at least 3 different voltages, memory compiler, from 3rd party, like TSMC or equivalent
Cadence Lab access to students for assigned Lab hours, with necessary compute infrastructure
Students should know CPU, Digital design and Verilog HDL as pre-requisite